CLAIMS

1. A composite capacitor in a semiconductor die, said composite capacitor comprising:

a lower electrode of a lower capacitor, said lower electrode of said lower capacitor situated in a lower interconnect metal layer in said semiconductor die;

an upper electrode of said lower capacitor, said upper electrode situated within a lower interlayer dielectric layer, said lower interlayer dielectric layer separating said lower interconnect metal layer from an upper interconnect metal layer;

a lower electrode of an upper capacitor, said lower electrode of said upper capacitor situated in said upper interconnect metal layer in said semiconductor die;

an upper electrode of said upper capacitor, said upper electrode situated within an upper interlayer dielectric layer, said upper interlayer dielectric layer being situated over said upper interconnect metal layer;

said upper electrode of said lower capacitor being connected to said lower electrode of said upper capacitor;

said lower electrode of said lower capacitor being connected to said upper electrode of said upper capacitor, whereby said composite capacitor is a parallel combination of said lower capacitor and said upper capacitor.

2. The composite capacitor of claim 1 wherein said upper electrode of said lower capacitor is connected to said lower electrode of said upper capacitor by at least one via.

3. The composite capacitor of claim 1 wherein said lower electrode of said lower capacitor is connected to said upper electrode of said upper capacitor by at least one via.

4. The composite capacitor of claim 1 further comprising a high-k dielectric situated between said lower and upper electrodes of said lower capacitor.

5. The composite capacitor of claim 4 wherein said high-k dielectric is selected from the group consisting of silicon oxide, silicon nitride, tantalum pentoxide, aluminum oxide, hafnium oxide, zirconium oxide, zirconium aluminum silicate, hafnium silicate, and hafnium aluminum silicate.

6. The composite capacitor of claim 1 further comprising a high-k dielectric situated between said lower and upper electrodes of said upper capacitor.

7. The composite capacitor of claim 6 wherein said high-k dielectric is selected from the group consisting of silicon oxide, silicon nitride, tantalum pentoxide, aluminum oxide, hafnium oxide, zirconium oxide, zirconium aluminum silicate, hafnium silicate, and hafnium aluminum silicate.

8. The composite capacitor of claim 1 wherein said lower and upper interlayer dielectric layers comprise a low-k dielectric.

9. The composite capacitor of claim 8 wherein said low-k dielectric is selected from the group consisting of porous silica, fluorinated amorphous carbon, fluoro-polymer, parylene, polyarylene ether, silsesquioxane, fluorinated silicon dioxide, and diamond-like carbon.

10. The composite capacitor of claim 1 further comprising:

a first metal segment situated in said upper interconnect metal layer, said first metal segment being connected to said lower electrode of said lower capacitor and to said upper electrode of said upper capacitor.

11. The composite capacitor of claim 10 wherein said first metal segment is connected to said lower electrode of said lower capacitor by at least one via.

12. The composite capacitor of claim 10 wherein said first metal segment is connected to said upper electrode of said upper capacitor by a plurality of vias and a second metal segment, said second metal segment being situated over said upper interlayer dielectric layer.

13. The composite capacitor of claim 1 wherein said upper electrode of said lower capacitor and said upper electrode of said upper capacitor comprise metal selected from the group consisting of titanium nitride and tantalum nitride.

14. A method for fabricating a composite capacitor in a semiconductor die, said method comprising steps of:

depositing a lower interconnect metal layer;

forming an upper electrode of a lower capacitor over said lower interconnect metal layer;

patterning said lower interconnect metal layer to form a lower electrode of said lower capacitor;

depositing an upper interconnect metal layer;

forming an upper electrode of an upper capacitor over said upper interconnect metal layer;

patterning said upper interconnect metal layer to form a lower electrode of said upper capacitor.

15. The method of claim 14 further comprising a step of connecting said upper electrode of said lower capacitor to said lower electrode of said upper capacitor by at least one via.

16. The method of claim 14 further comprising a step of connecting said lower electrode of said lower capacitor to said upper electrode of said upper capacitor by at least one via.

17. The method of claim 14 further comprising a step of forming a high-k dielectric between said lower and upper electrodes of said lower capacitor.

18. The method of claim 17 wherein said high-k dielectric is selected from the group consisting of silicon oxide, silicon nitride, tantalum pentoxide, aluminum oxide, hafnium oxide, zirconium oxide, zirconium aluminum silicate, hafnium silicate, and hafnium aluminum silicate.

19. The method of claim 14 further comprising a step of forming a high-k dielectric between said lower and upper electrodes of said upper capacitor.

20. The method of claim 19 wherein said high-k dielectric is selected from the group consisting of silicon oxide, silicon nitride, tantalum pentoxide, aluminum oxide, hafnium oxide, zirconium oxide, zirconium aluminum silicate, hafnium silicate, and hafnium aluminum silicate.

21. The method of claim 14 wherein said upper electrode of said lower capacitor and said upper electrode of said upper capacitor comprise metal selected from the group consisting of titanium nitride and tantalum nitride.

22. The method of claim 14 wherein said upper electrode of said lower capacitor and said upper electrode of said upper capacitor are fabricated utilizing a common mask.